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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,168	10/22/2001	Nai-Shung Chang	JCLA6880	4878

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,168	CHANG ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9 and 11-17* is/are rejected.

7)☒ Claim(s) *4-8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are presented for examination.

Claim Objections

2. Claim11 is objected to because of the following informalities: "said suspend status output signal" should be changed to "a suspend status output signal" to be consistent with claim 9. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polzin et al. (5,644,760) (hereinafter Polzin) in view of Robertson (6,529,967).

As to claim 1, Polzin teaches an apparatus for supporting multi-processors (processor cards), wherein said apparatus is coupled to a central processing unit socket, having a plurality of connecting pins (at least abstract, col. 3, lines 42-52, col. 6, lines 14-26, and col. 10, lines 52-65). However, Polzin does not explicitly disclose the socket connecting different types of processor cards with different voltages and a method to detect those types of processor cards. Robertson teaches socket connecting different types of cards with different voltages (3.3 volt, 5.0 volt) and a method to detect those types of cards including: when the socket is inserted with a first type card (e.g. 5.0 volt card), a first pin (102) among said connecting pins has a first equivalent resistance, and

when said socket is inserted with a second type card (e.g. 3.3 volt card), said first pins has a second equivalent resistance (col. 5 line 37 to col. 6 line 27); a distinguish device (control logic 110), coupled to said first pin to apply a difference between said first and said second resistance to generate a card select signal (3.3 volt enable or 5.0 volt enable) (Fig. 3); and a switch circuit (col. 7, lines 7-11), coupled to said distinguish device and said card socket to selectively connect a plurality of first type card signals to said corresponding connecting pins, and a plurality of second card signals to said corresponding connecting pins according to control of said card select signal (col. 3 line 56 to col. 5 line 64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to including detecting different types of card and a method to detect those types of card as taught by Roberson in the system of Polzin to allow cards having different voltages to be physically inserted into the same standard connector on the system board (col. 1, lines 8-17).

As to claim 2, Robertson further teaches when said CPU socket is inserted with said first type CPU, a second pin (101) among said connecting pins has a third equivalent resistance, and when said CPU socket is inserted with said second type CPU, said second pin has a fourth equivalent resistance, and said distinguish device is coupled to said second pin to use a difference between said first, second, third and said fourth equivalent resistance to determine a type of said CPU inserted in said CPU socket, and to generate a CPU select signal (Fig. 3 and col. 5 line 37 to col. 6 line 27).

As to claim 13, Robertson further teaches said distinguish device is supplied power from a prepared power supply (col. 7, lines 7-11).

4. Claims 3, 9, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polzin et al. (5,644,760) (hereinafter Polzin) in view of Robertson (6,529,967), and further in view of Kubo et al. (6,671,814) (hereinafter Kubo).

As to claim 3, the argument above for claim 2 applies. Robertson further teaches the distinguish device further comprises a processor select circuit (110), coupled to said first and said second pins to use a difference between said first, said second, said third, and said fourth equivalent resistances to generate a CPU select signal (col. 6, lines 1-27 and col. 7, lines 31-47). However, Polzin and Robertson do not explicitly disclose suspend status input signal wherein an interval control circuit receives said suspend status input signal and delays said suspend status input signal with a predetermine stop determination time, so that said processor select circuit cuts off said connection between said first pin and said processor select circuit. Kubo teaches receiving suspend status input signal (disconnection signal from a user) and delays said suspend status input signal with a predetermine stop determination time (after the lapse of a predetermined time), so that a select circuit cuts off the connection at the pins (disconnects the power supply line) (col. 5, lines 5-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include receiving suspend status input signal and delays said suspend status input signal with a predetermine stop determination time, so that a select circuit cuts off the connection at the pins as taught by Kubo in the system of Polzin and Robertson to reduce power consumption when the device is not used and prevent erroneous operation (col. 5, lines 26-42).

As to claim 9, the argument above for claim 1 applies. Robertson further teaches the distinguish device further comprises a processor select circuit (110), coupled to said first pin to use a difference between said first equivalent resistance and said second equivalent resistance to generate said CPU select signal (col. 6, lines 1-27 and col. 7, lines 31-47). However, Polzin and Robertson do not explicitly disclose suspend status input signal wherein an interval control circuit receives said suspend status input signal and delays said suspend status input signal with a predetermine stop determination time, so that said processor select circuit cuts off a connection between said first pin second pin and said processor select circuit. Kubo teaches receiving suspend status input signal (disconnection signal from a user) and delays said suspend status input signal with a predetermine stop determination time (after the lapse of a predetermined time), so that a select circuit cuts off the connection at the pins (disconnects the power supply line) (col. 5, lines 5-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include receiving suspend status input signal and delays said suspend status input signal with a predetermine stop determination time, so that a select circuit cuts off the connection at the pins as taught by Kubo in the system of Polzin and Robertson to reduce power consumption when the device is not used and prevent erroneous operation (col. 5, lines 26-42).

As to claim 11, Robertson further teaches coupled to a power regulator that provides a correct source voltage to said CPU inserted in said CPU socket according to a suspend status output signal (e.g. signal from gate 112) and said CPU select signal (e.g. signal from gate 116) (col. 7, lines 7-11).

As to claim 12, Kubo further teaches activate determination control circuit that enables said processor select circuit to operate after receiving said suspend status input signal (after stopping the operation of the device and then starting the operation of the device), so as to determine said type of said CPU inserted in said CPU socket (col. 4 line 61 to col. 5 line 42).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (5,76 1 ,479) (hereinafter Huang).

As to claim 14, Huang teaches a method for supporting multi-processors in a single motherboard, applied to a computer system (abstract) that comprises a CPU socket (e.g. socket 1001) and a suspend status input signal (CPURST, BREQ), wherein the CPU socket comprises a plurality of connecting pins (e.g. pin B14, S 10, A13, C14, . . .) (tables 2-3 and col. 20, lines l 7-67) of which a first pin (e.g. B 14) has a first equivalent resistance when a first type CPU is inserted in said CPU socket, and has a second resistance when said CPU socket is inserted with a second type CPU (col. 20, lines 25-28), said method comprising: using a difference between said first equivalent resistance and said second equivalent resistance to generate a CPU select signal (identification

signal) (col. 22, lines 54-63); and selectively connecting a plurality of first CPU signals to said corresponding connecting pins, and a plurality of second type CPU signals to said corresponding pins according to said CPU select signal (at least Fig. 10, and col. 20, lines 7-67).

As to claim 1 5, Huang further teaches delaying said suspend status input signal with a predetermined stop determination time after receiving (by timing control logic means U7), and determining which type of said CPU is inserted in said CPU socket within said predetermined stop determination time (col. 9 line 59 to col. 10 line 17).

As to claim 16, Huang further teaches delaying the suspend status input signal with a predetermined buffer time (by delay circuit U8) after the predetermined stop determination time to allow said CPU is inserted in said CPU socket operating normally (col. 9 line 59 to col. 10 line 17).

As to claim 1 7, Huang further teaches a second pin (e.g. A13, C14, S 10) among said connecting pins has a third equivalent resistance when said first type CPU is inserted in said CPU, and has a fourth equivalent resistance when said second type CPU is inserted in said CPU (col. 20 lines 65-67, col. 21 lines 24-67), and a difference between said third equivalent resistance and said fourth equivalent resistance is used to determined said type of said CPU inserted in said CPU socket (Figs. 10-1 1 and col. 22, lines 1-44).

Response to Arguments

6. Applicant's arguments with respect to claim the newly added limitation in claim 1 have been considered but are moot in view of the new ground(s) of rejection.

With respect to Applicant's argument on pages 14-15 of the Remarks that "Huang differs from the present invention as it uses *two different sockets* for supporting two different processors", it is noted that Huang discloses "the first socket 1001 is capable of receiving either the 80486DX or the 80487SX processor models" (col. 20, lines 17-24). Applicant further stated "the identification is not described as being based on *measuring the resistance* generated by each plugged in processor and finding out the difference between the *measured resistances*", again the features upon which applicant relies (e.g. *measuring the resistance)* are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim reads "a first pin has a first equivalent resistance when a first type CPU is inserted in said CPU socket, and has a second resistance...., using a difference between said first equivalent resistance and said second equivalent resistance to generate a CPU select signal". In this case, since pin B14 will be in contact with a 80487SX module when it is plugged in (providing MP# signal) or open when a 80486DX is plugged in (providing a high voltage) (col. 20, lines 42-59), thus the pin has a first equivalent resistance when a first type CPU is plugged in and has a second equivalent resistance when a second type is plugged in.

Allowable Subject Matter

7. Claims 4-8, 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses detecting insertion of a module by monitoring pin connection which changes its resistance, voltage or current and allow a sufficient time to insure that the module is properly seated in the connector:

US Patent 6,401,157 Nguyen et al.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

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PRIMARY EXAMINER